REMARKS

Introduction

Upon entry of the foregoing Response, claims 1-6 and 8-31 are pending in the application. No claims have been amended. No new matter is being presented.

In view of the following remarks, reconsideration and allowance of all the pending claims are respectfully requested.

Rejection under 35 USC §103

Claims 1-6 and 8-31 have been rejected under 35 U.S.C. §103(a) as being unpatentable over the applicant's admitted prior art (AAPA) in view of U.S. Patent No. 7,006,068 to Haga. Applicant respectfully traverses the rejection for at least the following reasons.

Independent claim 1

In the Office Action mailed on March 12, 2009, the Examiner contends that AAPA discloses most of the features of claim 1, except the Examiner acknowledges that AAPA does not explicitly disclose "a first inverter to invert the signal output from the level converter and a second inverter including at least two time extending elements to extend the inverted signal output from the first inverter by a transient time of the output potential level of the signal input from the level converter to the switching unit during which the potential level of the signal input from the level converter to the switching unit is converted from a first signal level to a second signal level and vice versa."

However, the Examiner relies on FIG. 5 of Haga as allegedly disclosing the features that are lacking in AAPA as applied to claim 1, and then concludes that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teachings of Haga into the AAPA," to arrive at all of the features recited in independent claim 1.

Applicant respectfully disagrees with the Examiner's allegations, and submits that Fig. 5 or any part of Haga fails to teach or suggest the features that are lacking in AAPA, for at least the following reasons.

Fig. 5 of Haga illustrates an arrangement having a sampling level converter circuit (refer to Fig. 1) connected to a CMOS inverter circuit 10. The Examiner relies on MP3 and MN5 as allegedly corresponding to Applicant's first inverter, and MP11-12 and MN11-12 as allegedly corresponding to Applicant's second inverter. However, Haga's MOS transistors MP11-12 and MN 11-12 do not "extend the inverted signal output from the first inverter by a transient time...of the signal inputted from the level converter," as recited in claim 1. In contrast, Haga's elements MP11-12 and MN 11-12 merely function as a "clocked inverter" to prevent clock skew with regard to the timing of the rising edge of the signal XSMP, which has nothing to do with "to extend the inverted signal output from the first inverter by a transient time...of the signal inputted from the level converter," as recited in independent claim 1. *See*, Haga, col. 15, lines 42-50.

For example, Haga states in col. 15, lines 45-52 that "even though the node N2 is at a high potential (10 V), the N-channel MOS transistor MN11 does not turn on and the output at the output terminal OUT does not fall to the low level (O V)." Nowhere does Haga's alleged "second inverter" include "at least two time extending elements to extend the inverted signal output from the first inverter by a transient time...of the signal inputted from the level converter," as recited in claim 1. At best, Haga's MOS transistors MP11-12 and MN 11-12 merely prevent the output terminal OUT from falling to a low level (0 V) under the presence of clock skew. *See,* Haga, col. 15, lines 46-53.

In fact, upon examination of Haga's circuit of Fig. 5, those skilled in the art would clearly appreciate that the only delay (e.g., time extension) in the operation of Haga's circuit results from a propagation delay time of the MOS transistors and a delay of the rising edge of signal XSMP. *See*, Haga, col. 16, lines 20-23. This is distinctly different than "a second inverter including at least two time extending elements to extend the inverted signal output from the first inverter by a transient time...of the signal inputted from the level converter," as recited in claim 1.

It is well-settled that "[t]o establish a *prima facie* case of obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Thus, since the Examiner has not shown that AAPA and Haga, separately or in combination, teach or suggest at least "a second inverter including at least two time extending elements to extend the inverted signal output from the first inverter by a transient time of the output potential level of the signal input from the level converter to the switching unit during which the potential level of the signal input from the level converter to the switching unit is converted from a first signal level to a second signal level and vice versa," these documents cannot be properly relied on to reject claim 1 under 35 U.S.C. §103(a) as submitted in the Office Action mailed on March 12, 2009, and withdrawal of the rejection and allowance of independent claim 1 are respectfully requested.

Moreover, it is respectfully submitted that one of ordinary skill in the art would not be motivated to modify Fig. 5 of Haga to arrive at Applicant's invention, for at least the reason that doing so would destroy the purpose and functionality of Haga, which is to prevent malfunction of the circuit under the presence of clock skew. For example, even if it would be possible to incorporate "time extending elements" into Haga's circuit in accordance with Applicant's invention, this would destroy the intended purpose of Haga's circuit, which is to prevent a malfunction due to a delay in the rising edge of signal XSMP (since the time extending elements would introduce additional delays besides the delay in the rising edge of the signal XSMP). As the Examiner is surely aware, "[r]eferences are not properly combinable or modifiable if their intended function is destroyed. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Thus, since Haga's circuit (Fig. 5) is designed to prevent malfunction of the circuit under the presence of clock skew, one of ordinary skill in the art would not have been motivated to modify Haga's circuit to include "at least two time extending parts least two time extending elements to extend the inverted signal output from the first inverter by a transient time...of the signal inputted from the level converter," as recited in independent claim 1, since this would mean disregarding an essential feature of Haga, which is to prevent malfunction due to a delay in the

rising edge of the signal XSMP.

Accordingly, Applicant respectfully submits that independent claim 1 is patentably distinguishable over AAPA and Haga, whether taken alone or in combination with one another, and withdrawal of the rejection and allowance of independent claim 1 are respectfully solicited.

Independent claims 6 and 8

With regard to independent claims 6 and 8, the Examiner relies on Fig. 5 of Haga and elements MP3, MN5, MP11-12 and MN11-12 as allegedly corresponding to all of the features that are lacking in AAPA as applied to these claims. However, as pointed out above in connection with independent claim 1, Haga's MOS transistors MP11-12 and MN 11-12 do not, among other things, "extend[] a first transient time of the output level of the inverted signal by a predetermined time in accordance with an output signal generating when the level of the inputted signal is converted, the transient time being a time period during which the level is converted from a first signal level to a second signal level," as recited in independent claim 6, and as similarly recited in independent claim 8.

In contrast, Haga's circuit merely functions as a "clocked inverter" to prevent clock skew with regard to the timing of the rising edge of the signal XSMP, which has nothing to do with "extending a first transient time of the output level of the inverted signal," as recited in the subject claims. *See*, Haga, col. 15, lines 42-50. For example, Haga states in col. 15, lines 45-52 that "even though the node N2 is at a high potential (10 V), the N-channel MOS transistor MN11 does not turn on and the output at the output terminal OUT does not fall to the low level (O V)." At best, Haga's MOS transistors MP11-12 and MN 11-12 merely prevent the output terminal OUT from falling to a low level (0 V) under the presence of clock skew. *See*, Haga, col. 15, lines 46-53.

In fact, upon examination of Haga's circuit of Fig. 5, those skilled in the art would clearly appreciate that the only delay (e.g., time extension) in the operation of Haga's circuit results from a propagation delay time of the MOS transistors and a delay of the rising edge of signal XSMP. *See*, Haga, col. 16, lines 20-23. This is distinctly different than "extending a first

transient time of the output level of the inverted signal by a predetermined time in accordance with an output signal generating when the level of the inputted signal is converted, the transient time being a time period during which the level is converted from a first signal level to a second signal level," as recited in independent claim 6, and as similarly recited in independent claim 8.

Moreover, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to modify Fig. 5 of Haga to arrive at Applicant's invention as recited in independent claims 6 and 8, for at least the reason that doing so would destroy the purpose and functionality of Haga, which is to prevent malfunction of the circuit under the presence of clock skew. For example, even if it would be possible to "extend a first transient time of the output level of the inverted signal" with Haga's circuit, this would destroy the intended purpose of Haga's circuit, which is to prevent a malfunction due to a delay in the rising edge of signal XSMP (since the time extending elements would introduce additional delays besides the delay in the rising edge of the signal XSMP). As the Examiner is surely aware, "[r]eferences are not properly combinable or modifiable if their intended function is destroyed. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Thus, since Haga's circuit (Fig. 5) is designed to prevent malfunction of the circuit under the presence of clock skew, one of ordinary skill in the art would not be motivated to modify Haga's circuit to include "extending a first transient time of the output level of the inverted signal by a predetermined time in accordance with an output signal generating when the level of the inputted signal is converted, the transient time being a time period during which the level is converted from a first signal level to a second signal level," as recited in the subject claims, since this would mean disregarding an essential feature of Haga, which is to prevent malfunction due to a delay in the rising edge of the signal XSMP.

Accordingly, Applicant respectfully submits that independent claims 6 and 8 are patentably distinguishable over AAPA and Haga, whether taken alone or in combination with one another, and withdrawal of the rejection and allowance of independent claims 6 and 8 are respectfully solicited.

Independent claim 31

With regard to independent claim 31, the Examiner relies on Fig. 5 of Haga and elements MP3, MN5, MP11-12 and MN11-12 as allegedly corresponding to all of the features that are lacking in AAPA as applied to independent claim 31. However, as pointed out above in connection with Applicant's other independent claims, Haga's MOS transistors MP11-12 and MN 11-12 do not, among other things, "first and second logic units to increase a time required to change the inverted nozzle selection signal between the logic high and the logic low," as recited in independent claim 31.

In contrast, Haga's circuit merely functions as a "clocked inverter" to prevent clock skew with regard to the timing of the rising edge of the signal XSMP, which has nothing to do with "increas[ing] a time required to change the inverted nozzle selection signal between the logic high and the logic low," as recited in independent claim 31. *See*, Haga, col. 15, lines 42-50. For example, Haga states in col. 15, lines 45-52 that "even though the node N2 is at a high potential (10 V), the N-channel MOS transistor MN11 does not turn on and the output at the output terminal OUT does not fall to the low level (O V)." At best, Haga's MOS transistors MP11-12 and MN 11-12 merely prevent the output terminal OUT from falling to a low level (0 V) under the presence of clock skew. *See*, Haga, col. 15, lines 46-53.

In fact, upon examination of Haga's circuit of Fig. 5, those skilled in the art would clearly appreciate that the only delay (e.g., time extension) in the operation of Haga's circuit results from a propagation delay time of the MOS transistors and a delay of the rising edge of signal XSMP. *See*, Haga, col. 16, lines 20-23. This is distinctly different than "increas[ing] a time required to change the inverted nozzle selection signal between the logic high and the logic low," as recited in independent claim 31.

Moreover, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to modify Fig. 5 of Haga to arrive at Applicant's invention as recited in independent claim 31, for at least the reason that doing so would destroy the purpose and functionality of Haga, which is to prevent malfunction of the circuit under the presence of clock skew. For example, even if it would be possible to "increase a time required to change the inverted nozzle selection signal between the logic high and the logic low" with Haga's circuit, this would destroy the intended purpose of Haga's circuit, which is to prevent a malfunction due

to a delay in the rising edge of signal XSMP (since the time extending elements would introduce additional delays besides the delay in the rising edge of the signal XSMP). As the Examiner is surely aware, "[r]eferences are not properly combinable or modifiable if their intended function is destroyed. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Thus, since Haga's circuit (Fig. 5) is designed to prevent malfunction of the circuit under the presence of clock skew, one of ordinary skill in the art would not be motivated to modify Haga's circuit to include "increas[ing] a time required to change the inverted nozzle selection signal between the logic high and the logic low," as recited in independent claim 31, since this would mean disregarding an essential feature of Haga, which is to prevent malfunction due to a delay in the rising edge of the signal XSMP.

Accordingly, Applicant respectfully submits that independent claim 31 is patentably distinguishable over AAPA and Haga, whether taken alone or in combination with one another, and withdrawal of the rejection and allowance of independent claim 31 are respectfully solicited.

Dependent Claims 2-5 and 9-30

With respect to claims 2-5 and 9-30, it is respectfully submitted that for at least the reason that claims 2-5 and 9-30 depend from one of independent claims 1 and 8, which are patentably distinguishable from AAPA and Haga for at least the reasons provided above, and therefore contain each of the features as recited in independent claims 1 and 8, dependent claims 2-5 and 9-30 are also patentably distinguishable from AAPA and Haga, and withdrawal of this rejection and allowance of these claims are respectfully solicited.

Examiner's Response to Arguments

On page 21 of the Office Action mailed on March 12, 2009, the Examiner states that "Applicant's arguments with respect to claims 1-6 and 8-31 have been considered but are moot in view of the new ground(s) of rejection." In particular, the Examiner states that "[t]he applicant's arguments filed on 02/04/09 were persuasive with respect to figure 9 of Haga, as previously cited by the examiner. However, the new rejection above is based on figure 5 of

Haga."

In the above Remarks, Applicant respectfully submits that the Examiner's rejections set forth on pages 2-20 of the Office Action have been fully addressed and overcome. Accordingly, reconsideration of the pending claims in view of the above Remarks is earnestly solicited.

Conclusion

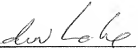
It is respectfully submitted that a full and complete response has been made to the outstanding Office Action and, as such, there being no other objections or rejections, this application is in condition for allowance, and a notice to this effect is earnestly solicited.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided below.

If any further fees are required in connection with the filing of this amendment, please charge the same to our Deposit Account No. 502827.

Respectfully submitted,

STANZIONE & KIM, LLP

Dated: June 9, 2009
By: 
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